Compact Broadband Filters for Hybrid Circuits using Flip-Chip-Technology

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***Abstract*— A compact broadband filter is presented. The design is based on a microstrip substrate wherein half of the filter is located on a thinfilm chip and mounted in flip-chip fashion. Revealing a fractional bandwidth of as much as 50% and a measured insertion loss less than 1.5 dB at 20 GHz, the required real-estate remains small compared to state-of-the-art designs. Exemplarily, a hybrid K-Band doubler and buffer-amplifier were realized solely using flip-chip-technology in conjunction with the developed filters. Measured results agree very well with predictions from commercial software tools.**

I. Introduction

Planar, ceramic based microwave circuits are widely used in communication systems. Especially in high end applications such as satellite communications, they are preferred for reliability reasons, facile processing and small feature sizes as little as 10 μm by means of photolithography. Low Temperature Cofired Ceramics (LTCC) on the other hand allows the implementation of complex, though very compact RF-circuits in a multilayer substrate. While this technology is well known from mass market applications, the resolution in standard processes cannot be smaller than 100 μm.
In the presented approach, we extend a standard planar alumina substrate to a quasi multi-layer substrate by using flip-chip technology. Thus, this concept confines the advantages of both planar substrates and multilayer LTCC technology. Exemplarily, we verify this approach on vertical microwave filters. The design goals are a small size, low insertion loss, low return loss and a broadband transfer function, which inhibits DC current conduction from input to output port. This filter type can e.g. serve as a DC-block in order to separate two active stages on the bias level, where planar, interdigital capacitors [1] or coplanar quarter wave couplers [2] were utilized in the past. In the following, a detailed discussion is presented also covering the impact on manufacturing and placement tolerances.

II. Flip-Chip Filter Geometries

The general concept of the developed filters is portrayed in Fig. 1: A microstrip alumina substrate contains one part of the filter structure. A second part is located on a chip without any back-metallization. Thus coupling occurs between both substrate and chip layer. The distance between chip and substrate is adjusted using appropriate gold stud bumps, which not only serve as electrical interconnects but also improve mechanical stability. The bumps in our filters were generated by means of a manual ball bonder (*Hybond*) using optical alignment procedures. The repeatability was determined to be approximately 10 μm for lateral positioning. The attachment has been accomplished using thermocompression tools and a *Finetech* fineplacer with a placement accuracy of 5 μm according to the manufacturers specification. The mounting profile of the chip was a linear temperature ramp of 7 °K/s and a force of 1.0 N/bump.

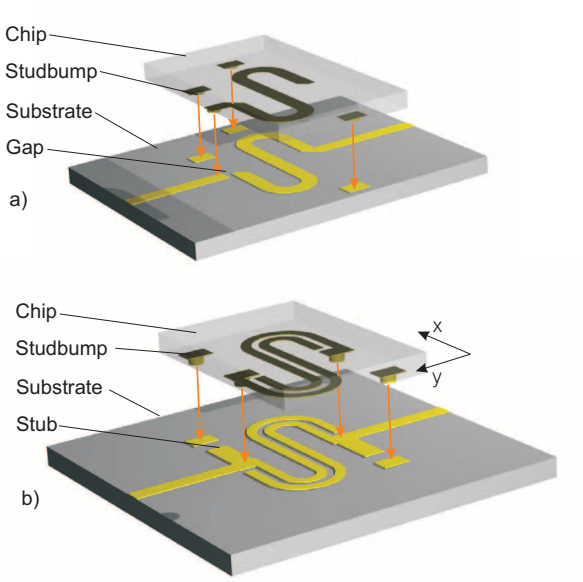

Fig. 1. Illustration of the vertically coupled line flip-chip filter (a) and broadband interdigital flip-chip filter (b): Part of the filter structure is located on the microstrip substrate, while the other part is added by mounting a small chip without backside metallization.

A. Vertically Coupled Line Filter

A first investigated structure is a quarter wavelength vertically coupled line filter as illustrated in Fig. 1 (a). The line on the bottom substrate is equipped with a gap and the counterpart on the chip overlaps the meander in the same way. This quarter wavelength coupled line section is arranged in a *S*-shape for optimally occupying the real estate. The structure has been simulated and optimized using a 3D-software [3] and realized on alumina substrate with a nominal thickness of 127 μm and a stud bump height of 20 μm. The realized test vehicle is shown in Fig. 2 together with measured and simulated results. The filter enables a very broad band of transmission with an upper resonance slightly above 40 GHz, which is determined by the

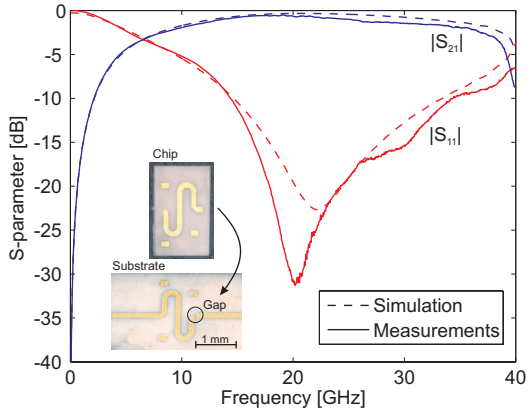

Fig. 2. Results of a 20 GHz center frequency vertically coupled line filter in flip-chip-technology. The stud bump height is approximately 30 μm. The inset shows designed test structures on alumina substrate.

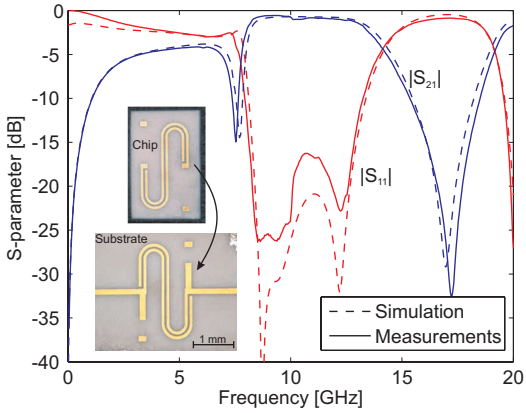

Fig. 4. Results of a 10 GHz center frequency flip-chip-filter with a stud bump height of approx. 60 μm. The inset shows designed test structures on alumina substrate.

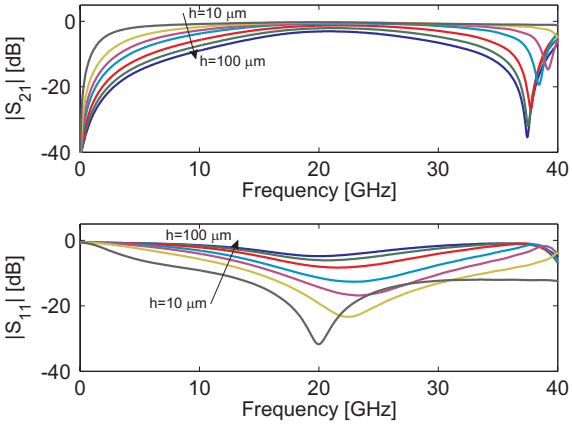

Fig. 3. Simulation results of the vertically coupled line filter for stud bump heights from 10 μm to 100 μm.

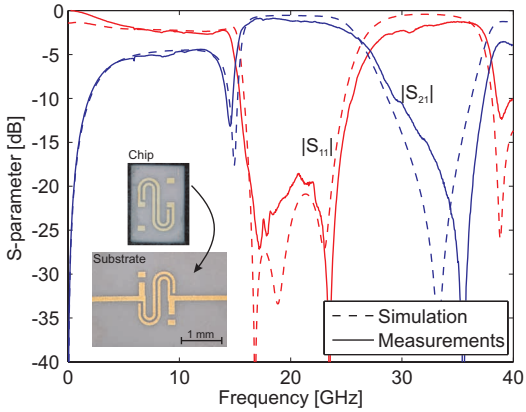

Fig. 5. Results of a 20 GHz center frequency flip-chip-filter with a stud bump height of approx. 60 μm. The inset shows designed test structures on alumina substrate.

overlap length.

The influence of the stud bump height on the filter characteristic was studied in the simulation programm. Results of this analysis for a fixed coupled line width of 100 μm are displayed in Fig. 3. Reducing the distance between chip and substrate increases the mutual capacitance between the vertically coupled lines, thus a general improvement in the transfer function is observed. In a physical structure, the final bump height is determined by its size before compression and the applied force. In our case, a height of 20 μm could be conveniently reached. The repeatability is mainly determined by machine parameters that allow sufficiently tight control here.

B. Broadband Interdigital Filter

A second investigated structure is shown in Fig. 1 (b). The vertically coupled lines were extended by also introducing lateral coupling. A stub was added to improve the flatness in the passband region. Here, the stud bump height was chosen to 60 μm. Measured results for a 10 GHz center frequency filter are displayed in Fig. 4 together with the predictions of the software. Excellent agreement is revealed over the entire range with a passband from 8 to 13 GHz. The measured insertion loss is about 0.8 dB at center frequency.

Scalability of this type of filter was evaluated by a second filter, this time at a center frequency of 20 GHz, with a flat passband from 16 to 24 GHz. An insertions loss of 1.1 dB was measured showing a slight increase towards higher frequencies. While the agreement between simulations and measurements is excellent below 20 GHz, the software underestimates losses above this frequency. We attribute this effect to the surface roughness of the conductors and the ceramics as well as to the contact resistances, which can not be modeled in the software. Corresponding test vehicles are depicted in the insets in Figs. 4 and 5.

As in the previously proposed structure, a parameter study in simulations was utilized to gain knowledge of the influence of manufacturing tolerances on the filter performance. As seen in Fig. 6, an increase in height decreases the fractional bandwidth, while all deviations from 60 μm target height

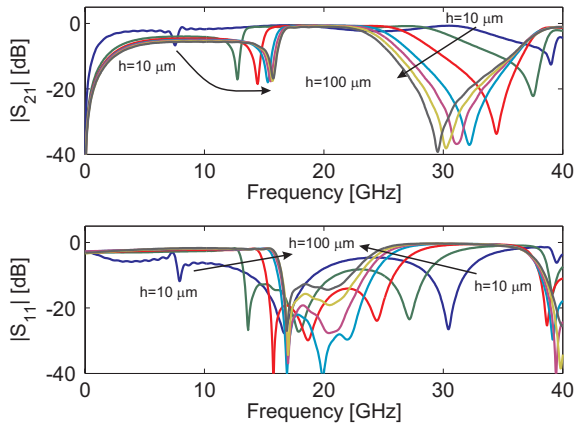

Fig. 6. Simulation results of the broadband interdigital filter for stud bump heights from 10 μm to 100 μm.

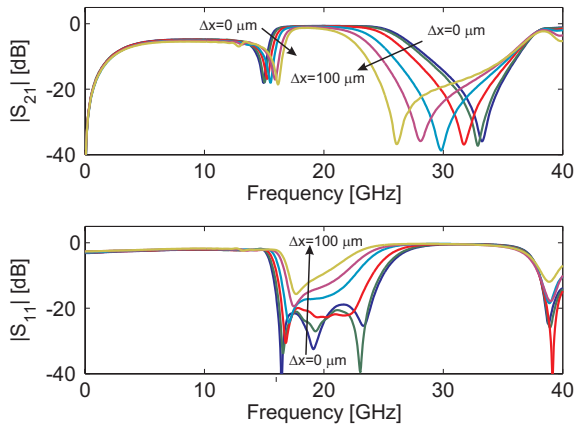

Fig. 7. Simulated placement tolerance analysis for a displaced chip by Δx from the ideal position relative to the substrate.

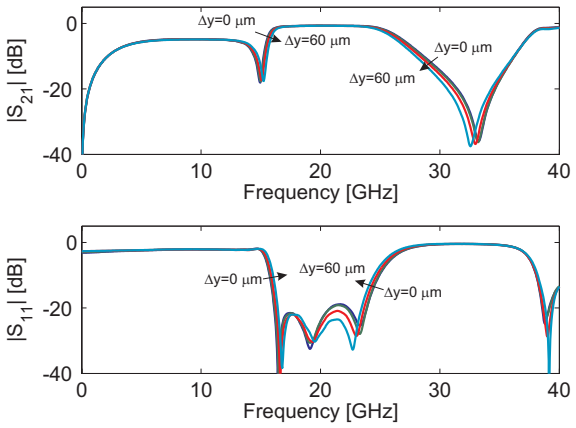

Fig. 8. Simulated placement tolerance analysis for a displaced chip by Δy from the ideal position relative to the substrate

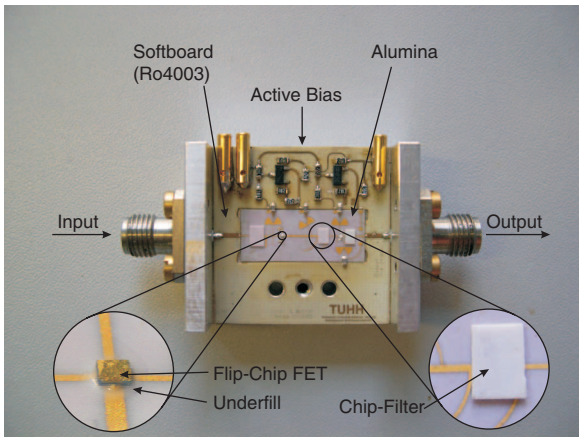

Fig. 9. Used package style for evaluating the designed hybrid circuits: A softboard (Ro4003) hosting active bias electronics and connections to the SMA-connectors is framing the hybrid circuit designed on alumina substrate. The chip components were exclusively mounted in flip-chip-technology using thermo-compression techniques.

increase the input reflection.

Secondly, lateral placement tolerances (see Fig. 1 (b) for coordinate conventions) were investigated as shown in Figs. 7 and 8 in 20 μm increments. For symmetry reasons, displacement in only positive directions needs to be considered. An offset in x-direction decreases the transmission bandwidth, while the input reflection increases. Up to a displacement of Δx = 40 μm, the filter performance is only little affected. Similar tendencies can be seen in the results for y-displacements, which were simulated up to Δy = 60 μm. Any larger value would cause the bumps to short the lateral coupled lines, which entirely changes the filter function. Yet the sensitivity to y-displacement is much lower as compared to x-displacements, since the *S*-shaped coupled line sections mostly take course in the same direction as the displacement. Within the simulated range no significant change is observed.

III. Hybrid Circuit Designs

In this work, we exclusively used flip-chip technology on a thinfilm alumina substrate (h=127 μm), as shown in Fig. 9.

In order to facilitate biasing of the circuits, an active biasing network was employed as proposed in [4], located on one side of the soft-substrate. The used transistor is a discrete low noise pHEMT (*EPB018A5* of *Excelics Seminconductor*) that was mounted and simulated in a flip-chip fashion by modifying bond-inductances and bond pad capacitances in the manufacturers model. The chip dimensions are 290x320 μm wherein the smallest pad is 60x68 μm, thus the placed stud bumps must not exceed 50 μm in diameter in order to provide a margin for compression. The chip was mounted in the same way as the filters, not exceeding 300 °C (maximum temperature as per manufacturer).

The first here presented circuit is a frequency doubler for input signals around a center frequency of 10 GHz (see Fig. 10 (a) for layout details). It is based on a single FET design operated in the vicinity of the transistors pinch-off region. For the core design, a reflector type topology was adapted [5]: Two filters are located at the gate and the drain terminals,

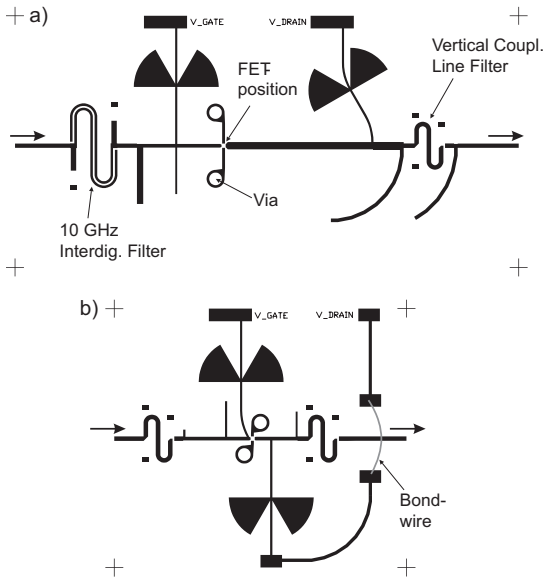

Fig. 10. Layouts of the designed circuits on Al_2O_3 substrate with thickness of 127 μm: a) X-Band/K-Band doubler and b) K-Band buffer amplifier (designs are shown without mounted chips).

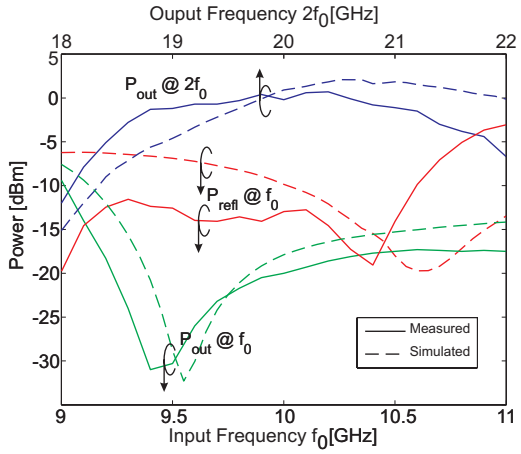

Fig. 11. Measured and simulated output power of the leaking fundamental, the desired first harmonic and the reflected power at the input terminal. The circuit was driven with a constant input power of 4 dBm at f_0.

wherein the filter at the gate contact is transparent for signals at the fundamental frequency f_0 but reflects the generated harmonic $2f_0$ and vice versa for the drain terminal. In our case, the presented vertically coupled line filter could be directly inserted in the output reflection network (see layout), thus improving miniaturization of the circuit. Both measured and simulated results for the developed circuit are shown in Fig. 11. The frequency sweep shows some inconsistency in the reflected power, which in turn impacts the conversion efficiency. We attribute this observation to uncertainties in the transistor model, which are known to occur especially at bias points close to pinch-off. The second herein presented circuit is a single FET amplifier (for layout see Fig. 10 (b)), which was designed for buffering signals of the proposed doubler or Ka-Band VCOs in general. The FET is biased at a drain

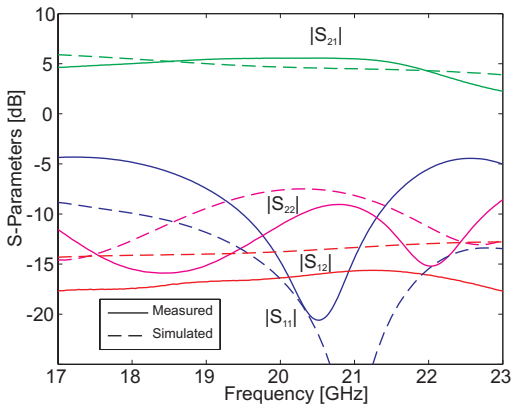

Fig. 12. Measured and simulated scattering parameters of the designed buffer K-band amplifier.

current of I_{DS}=25 mA. This circuit solely uses the coupled line filters as DC-blocks, which especially at the gate side help to achieve stable operation. According to the results shown in Fig. 12, the forward gain of approximately 5 dB, the reverse isolation and output matching perform equal or even better than simulated. Again the input reflection is increased as in the application of the doubler before.

IV. Conclusions

Multilayer filters utilizing planar substrate technology were realized by means of flip-chip interconnects. Measured results and simulations of the presented prototypes agree very well, revealing a low insertion loss between 0.7 and 1.1 dB at center frequency. A placement tolerance analysis showed, that uncertainties associated with the manufacturing equipment has only a minor impact on the performance. The functionality of the filters could be successfully demonstrated in two active circuits. The proposed method appears to be a useful alternative to realize multilayer circuits on planar substrates, where true multilayer technology cannot be applied.

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