A GaAs Distributed Amplifier with more than $7 \mathrm{V}_{\mathrm{pp}}$ Output for 40 GBit/s Modulators

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\textbf{Abstract} — In this paper, we report about a Distributed Amplifier (DA) with high output voltage swing sufficient to drive 40 GBit/s LiNbO\textsubscript{3} based Mach-Zehnder modulators. The amplifier was fabricated in a commercially available 150 nm GaAs power pHEMT technology. Measurements show a gain of 16 dB with an associated bandwidth of 40 GHz. For the 20 GHz fundamental, output power at the -1 dB gain compression point equals 21.7 dBm or $7 \mathrm{V}_{\mathrm{pp}}$.

\section{I. INTRODUCTION}

The increase of data communication in recent years demands for increasing bandwidth of the transmission systems. The driving motivation for an increasing bit rate is a reduced cost per bit. At lower bit-rates upgrading to four times the speed typically resulted in only 2.5 times the cost \cite{1}. In fiber communication systems, speed per channel increased from 2.5 Gbit/s (OC-48) to 10 Gbit/s (OC-192) and future 40 Gbit/s (OC-768) are examined. With very advanced transistor technologies, also first results are published for 80 Gbit/s \cite{2} and even 100 Gbit/s \cite{3}.

In case of 40 Gbit/s systems, the modulator driver is very challenging, because it simultaneously has to achieve a high output voltage swing of typically $5$ to $7 \mathrm{V}_{\mathrm{pp}}$ \cite{4} and a bandwidth exceeding 30 GHz. The increasing speed of silicon based technologies like SiGe, BiCMOS, or CMOS fulfill the bandwidth requirements for high bit-rate optical communication at low cost. For example SiGe HBTs with an $f_t$ of 350 GHz \cite{5} and SOI CMOS with up to 243 $f_t$ \cite{6} have been reported. However, increasing transistor speed is mainly achieved by strong lateral scaling which degrades breakdown voltage.

While InP based HBTs are the ideal candidate for high power applications at high frequencies \cite{4}, GaAs based circuits offer slightly degraded performance but with an advantage in terms of cost-effective production.

For the circuit concept, a distributed amplifier topology is chosen. The concept of distributed amplification has been around for over a half century \cite{7} and is one of the most used concepts in optical communication due to its excellent bandwidth performance. The idea of a DA is to split one large device into several small ones and to compensate for parasitic capacitances by high characteristic impedance transmission lines. The resulting small signal structure at the input and output of the DA is designed to behave like a 50 \Omega artificial transmission line and therefore shows both, small input and output reflections as well as flat gain over a large bandwidth. This makes a DA concept very attractive for 40 GBit/s circuits. Especially, the superposition of the signals on the drain line is ideally suitable to achieve high output power and therefore meet the requirements for driving a LiNbO\textsubscript{3} modulator.

\section{II. CIRCUIT DESIGN}

The amplifier is realized in the commercially available PPH15 process of United Monolithic Semiconductors (UMS). This is a high power 150 nm pseudomorphic GaAs HEMT process with an $f_t$ of 75 GHz. The devices have an optimum transconductance of $g_{m,\text{max}} = 550 \mathrm{mS/mm}$ at $V_{\text{GS}} = -0.4 \mathrm{V}$, a breakdown voltage of $V_{\text{BSD}} > 8 \mathrm{~V}$, and a power density of $P_{-1\text{dB}} = 0.6 \mathrm{~W/mm}$.

A DA with 6 stages was designed and the basic topology is shown in Fig. 1.

![Fig. 1. The amplifier consists of 6 cascode stages. A resistor at the second gate together with source degeneration are used to enable stability of the amplifier.](image)

Within the stages, cascode cells are used. Compared to a transistor in common source configuration a cascode provides several advantages:

- Unilateralization
- Possibility for gain variation
- Reduced Miller-effect
- Improved output resistance

A reduced Miller-effect decreases the input capacitance and thereby enhances the cut-off frequency of the artificial gate line. In case of DA design, the output conductance of the active device is essential, because it determines the attenuation and thereby the cut-off frequency. At frequencies close to DC parasitic output capacitance of a FET can be neglected, yielding an output resistance of the cascode equal to:

$$\Re\{Z_{\text{22}}\} \approx 2 \cdot r_{\text{ds}} + g_{m2} \cdot r_{\text{ds}}^2. \quad (1)$$

For high frequencies the cascode shows a negative resistance at its output terminal. Neglecting output conductance of the transistors ($g_{\text{ds1}} = g_{\text{ds2}} = 0$), the real part of the output impedance is:

$$\Re\{Z_{\text{22}}\} \approx \frac{g_{m2}}{\omega^2 (C_{\text{ds1}} + C_{\text{gs2}}) C_{\text{ds2}}}, \quad (2)$$
where $g_{m2}$, $C_{gs2}$, and $C_{ds2}$ are the transconductance, input capacitance, and output capacitance of the common gate transistor, $C_{ds1}$ is the output capacitance of the common source transistor.

The negative resistance is used to compensate for losses on the artificial drain line and thereby, enhances cut-off frequency. However, a negative output resistance also gives rise to instabilities and is partly compensated by the resistor $R_{2G}$ and inductive source degeneration, $Z_{FB}$. Other possibilities for stabilization of the DA are shown for example in [8], [9]. In order to have high voltage amplification, one can either use a large gate width for each stage or a large number of stages. While the first decreases cut-off frequency, the latter makes the amplifier more sensitive to process variations and typically decreases gain flatness. In this case the circuit is rather optimized for good gain flatness than cut-off frequency. Therefore the gate width is chosen relatively large (100 µm), enabling high gain within 6 stages. Even with this large device size simulated cut-off frequency of 42 GHz showed sufficient margin to fulfill the frequency requirements after process variations.

The corresponding layout of the circuit is shown in Fig. 2.

![Fig. 2. Layout of the distributed amplifier (chip size: 2.38 × 0.83 mm²)](image)

The large pad on the left hand side is used for external bias decoupling. For the measurements, a 100 nF SMD capacitor is glued on that pad to enable bias decoupling down to very low frequencies. Because parasitics of this capacitor would degrade high frequency performance of the amplifier, down to frequencies of approximately 5 GHz bias decoupling is made on-chip. A detailed schematic for this circuitry is shown in Fig. 3.

![Fig. 3. Termination for the reverse traveling wave. Bias-decoupling of frequencies higher 5 GHz is done on-chip. A pad is provided to directly attach a SMD capacitor on top of the chip.](image)

Parasitics due to physical connections to the capacitors, together with the capacitances itself result in resonances. This is attenuated by resistors. Additionally, the values for these resistors are chosen to compensate for gain ripples. Fig. 4 shows a micrograph of an external capacitor mounted on top of the amplifier.

![Fig. 4. Micrograph of an external SMD capacitor mounted on top of the GaAs-MMIC.](image)

III. MEASUREMENT RESULTS

All measurements were performed with a drain biasing of 8.0 V, a second gate voltage of 3.7 V and a gate source voltage of -0.3 V. This bias point gives a good compromise between small signal and power performance. The total DC-power consumption equals 1.6 W. On-wafer small signal measurements of this amplifier are shown in Fig. 5.

![Fig. 5. Measured small signal parameters of the amplifier. Gain equals 16 dB at DC with a corresponding bandwidth of 40 GHz. The gain equals to 16.0 dB with a corresponding cut-off frequency of 40 GHz. Up to 37 GHz the frequency response is very flat with gain-ripples of less than ±0.5 dB. However, a resonance at approximately 10 GHz degrades gain by nearly 2 dB. The resonance is due to the cascode cell itself, which is verified by measurements on a test structure. While this resonance degrades small signal performances, it does not degrade overall stability of the amplifier. Input matching is better than -8 dB up to 30 GHz, except for the frequency band between 9 and 10 GHz. Output matching is lower -10 dB up to 37 GHz. The output power performance versus frequency at the 1dB gain compression point is shown in Fig. 6. The output power equals to approximately 22 dBm at 0.5 GHz and is in very good agreement with simulations up to 10 GHz. However, at the 20 GHz fundamental measured output power equals 21.7 dBm which is more than 2 dB less than simulated.](image)
IV. SUMMARY

In this paper, we presented a distributed amplifier with a gain of 16.0 dB and a cut-off frequency of 40 GHz. Gain ripples are within $\pm0.5$V up to 37 GHz. Output power at the 20 GHz fundamental equals 21.7 dBm. This makes the amplifier capable for driving 40 Gbit/s LiNbO$_3$ modulators which require voltage swings up to 7V$_{pp}$.

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REFERENCES


